IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

KERANOS, LLC	§	
	§	
v.	§	Case No. 2:13-cv-17
	§	
SILICON STORAGE TECHNOLOGY, INC., et al.	§	

KERANOS, LLC	§	
	§	
v.	§	Case No. 2:13-cv-18
	§	
ANALOG DEVICES, INC.	§	

MEMORANDUM OPINION AND ORDER

On December 12, 2012, the Court held a hearing to determine the proper construction of the disputed claim terms in U.S. Patent No. 4,795,719, U.S. Patent No. 4,868,629, and U.S. Patent No. 5,042,009. On January 8, 2013, the Court entered a Provisional Opinion and Order providing the Court's constructions. The Court now enters this memorandum opinion and order setting forth the reasoning behind the Court's constructions.[1]

[1] This patent infringement action originated as a series of five related cases, including four declaratory judgment actions transferred to this district from the Northern District of California. In December 2012, the Court held a claim construction hearing followed by a status conference to address scheduling the remaining issues. Following the status conference, the Court realigned the cases so that the claims involving the manufacturing defendants were assigned to one case (2:13-cv-17) and the claims involving the customer defendants were assigned to another case (2:13-cv-18). The Court then entered separate schedules in each of the cases.

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I. BACKGROUND

Plaintiff brings suit alleging infringement of U.S. Patent Nos., 4,795,719 (the ’719 Patent), 4,868,629 (the ’629 Patent), and 5,042,009 (the ’009 Patent). The’719 Patent issued on January 3, 1989, the ’629 Patent issued on September 19, 1989, and the ’009 Patent issued on August 20, 1991.

The ’719 Patent—titled Self-Aligned Split Gate EPROM Process—and the ’629 Patent—titled Self-Aligned Split Gate EPROM—relate to a parent application filed on May 15, 1984. The claimed invention of these two patents is a memory cell with a split gate transistor, which includes a floating gate and a control gate. The floating gate is aligned with the drain region thus precisely defining the channel portion. The’629 Patent claims the memory cell having the split gate transistors, and the ’719 Patent claims the process for making the memory cells.

The ’009 Patent is titled Method for Programming a Floating Gate Memory Device and claims priority to an application filed on December 9, 1988.

II. CLAIM CONSTRUCTION PRINCIPLES

Claim construction is a matter of law. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995). The purpose of claim construction is to resolve the meanings and technical scope of claim terms. *U.S. Surgical Corp. v. Ethicon, Inc.*, 103 F.3d 1554, 1568 (Fed. Cir. 1997). When the parties dispute the scope of a claim term, “it is the court’s duty to resolve it.” *O2 Micro Int’l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1362 (Fed. Cir. 2008).

The claims of a patent define the scope of the invention. *Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1324 (Fed. Cir. 2002). They provide the “metes and bounds” of the patentee’s right to exclude. *Corning Glass Works v. Sumitomo Elec. U.S.A., Inc.*, 868 F.2d 1251, 1257 (Fed. Cir. 1989). Accordingly, claim construction begins with and “remain[s] centered on

the claim language itself." *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1116 (Fed. Cir. 2004).

Claim terms are normally given their "ordinary and customary meaning." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)). Generally, "the ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention." *Id* at 1313.

The best guide for defining a disputed term is a patent's intrinsic evidence. *Teleflex*, 299 F.3d at 1325. Intrinsic evidence includes the patent's specification and the prosecution history. *Id.*

The claims are part of the specification. *Markman*, 52 F.3d at 979. "[T]he context in which a term is used in the asserted claim can be highly instructive." *Phillips*, 415 F.3d at 1314; *see also Abtox, Inc. v. Exitron Corp.*, 122 F.3d 1019, 1023 (Fed Cir. 1997) ("[T]he language of the claim frames and ultimately resolves all issues of claim interpretation."). "Differences among claims can also be a useful guide in understanding the meaning of particular claim terms." *Phillips*, 415 F.3d at 1314.

In addition to the claims, the specification's written description is an important consideration during the claim construction process. *See Vitronics Corp.*, 90 F.3d at 1582. The written description provides further context for claim terms and may reflect a patentee's intent to limit the scope of the claims. *See Watts v. XL Sys., Inc.*, 232 F.3d 877, 882 (Fed. Cir. 2000). "[T]he specification 'is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.'" *Phillips*, 415 F.3d at 1315 (quoting *Vitronics*, 90 F.3d at 1582).

The specification may also resolve ambiguous claim terms "where the ordinary and accustomed meaning of the words used in the claims lack sufficient clarity to permit the scope of the claim to be ascertained from the words alone." *Teleflex, Inc.*, 299 F.3d at 1325. For example, "[a] claim interpretation that excludes a preferred embodiment from the scope of the claim 'is rarely, if ever, correct.'" *Globetrotter Software, Inc. v. Elam Computer Grp., Inc.*, 362 F.3d 1367, 1381 (Fed. Cir. 2004) (quoting *Vitronics Corp.*, 90 F.3d at 1583).

But care must be taken to avoid unnecessarily reading limitations from the specification into the claims. *Teleflex*, 299 F.3d at 1326; *see also Raytheon Co. v. Roper Corp.*, 724 F.2d 951, 957 (Fed. Cir. 1983) ("That claims are interpreted in light of the specification does not mean that everything expressed in the specification must be read into all the claims."). "[P]articular embodiments appearing in the written description will not be used to limit claim language that has broader effect." *Innova/Pure Water*, 381 F.3d at 1117; *see also Phillips*, 415 F.3d at 1323 ("[A]lthough the specification often describes very specific embodiments of the invention, we have repeatedly warned against confining the claims to those embodiments.").

The prosecution history is also part of the intrinsic evidence. *Phillips*, 415 F.3d at 1317. It "consists of the complete record of the proceedings before the PTO and includes the prior art cited during the examination of the patent." *Id.* "As in the case of the specification, a patent applicant may define a term in prosecuting a patent." *Home Diagnostics, Inc. v. LifeScan, Inc.*, 381 F.3d 1352, 1356 (Fed. Cir. 2004). Statements made during the prosecution of the patent may limit the scope of the claims. *Teleflex*, 299 F.3d at 1326; *see Omega Eng'g Inc. v. Raytek Corp*., 334 F.3d 1314, 1323 (Fed. Cir. 2003) (explaining that the doctrine of prosecution disclaimer "preclud[es] patentees from recapturing through claim interpretation specific meanings disclaimed during prosecution").

Finally, the Court may rely on extrinsic evidence to aid with understanding the meaning of claim terms. *Markman*, 52 F.3d at 981. Extrinsic evidence includes "all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises." *Id.* at 980. Extrinsic evidence is generally less useful or reliable, *Phillips*, 415 F.3d at 1317, and it should not be relied on when it contradicts the intrinsic evidence, *Markman*, 52 F.3d at 981.

III. CONSTRUCTION OF AGREED TERMS

The parties have agreed to the construction of the following terms:

Claim Term/Phrase/Clause: Claim No(s).	Agreed Definition
photoresist U.S. Patent No. 4,795,719 (claims 1, 7)	a light sensitive material used in semiconductor fabrication
said photoresist pattern U.S. Patent No. 4,795,719 (claim 1)	the antecedent "photoresist pattern" as defined by the Court
photoresistive coating U.S. Patent No. 4,795,719 (claim 7)	a covering of photoresist material
the coating U.S. Patent No. 4,795,719 (claim 7)	the antecedent "photoresistive coating" as defined by the Court
EPROM array U.S. Patent No. 4,868,629 (claim 5)	an arrangement of nonvolatile memory cells which can be programmed and erased

In view of the parties' agreements on the proper construction of these terms (2:10-cv-207, Doc. No. 691), the Court adopts the parties' agreed constructions.

IV. CONSTRUCTION OF DISPUTED TERMS

The parties' dispute focuses on the meaning and scope of 14 terms or phrases in the patents in suit. Having considered the parties' briefing and argument during the claim construction hearing, the Court construes the disputed terms as outlined below.

A. "at least a portion of"

Disputed Claim Term	'009	'719	'629	Plaintiff's Proposed Construction	Defendants' Proposed Construction
at least a portion of	1, 2, 4, 7, 8, 27, 28			some but not all	any portion of up to and including the whole

This term appears twice in Claim 1 of the '009 Patent. Thus, construction of this term directly impacts the scope of each claim that depends on Claim 1 (Claims 2, 4, 7, 8, 27, and 28). The parties' dispute pertains to whether this term limits Claim 1 to "split-gate" technology as Plaintiff claims or if it also encompasses "stacked gate" technology or other non-split-gate transistors, as Defendants contend. For the reasons discussed below, the Court adopts Defendants' proposed construction: "any portion of up to and including the whole."

1. The Claim Language

Claim 1 of the '090 Patent recites the following:

> A method for programming a floating gate transistor, said floating gate transistor comprising a source, a drain spaced apart from said source, said source and drain being of first conductivity type and formed in a semiconductor region of a second conductivity type, a channel extending between said source and drain, a floating gate extending over **at least a portion of** said channel, and a control gate extending over **at least a portion of** said floating gate, said method comprising the steps of:
>
> applying a programming voltage to said drain and control gate sufficient to cause hot electron injection programming of said transistor; and
>
> ensuring that the programming drain current for said transistor is less than a predetermined value.

(emphasis added).

2. Court's Construction

Defendants argue that Plaintiff reads "at least a portion of" to mean "*only* a portion of,"

which is inconsistent with the plain meaning of the term. Plaintiff counters that Defendants' construction renders the term meaningless as it encompasses *anything* over the floating gate or channel, whether completely over or only partially over. According to Plaintiff, the same effect would be accomplished by simply removing the disputed term from the claim language. The Court agrees with Defendant that the plain language of the term "at least" can include being over the entire channel or floating gate.

Plaintiff also emphasizes that multiple embodiments in the '009 Patent depict split-gate cell structure. *See, e.g.*, Fig. 1. Defendants counter that Fig. 12 illustrates a non-split-gate embodiment. Plaintiff responds that the Fig. 12 is not an embodiment but is instead used to demonstrate the problem corrected by the invention.

Although the Court agrees that Fig. 12 does not present an embodiment of the invention, *see* the'090 Patent, col. 8:36–45, Plaintiff's attempt to limit the scope of the claim to the preferred embodiments is without merit. *Electo Med. Sys., S.A. v. Cooper Life Scis., Inc.*, 34 F.3d 1048, 1054 (Fed. Cir. 1994) ("[A]lthough the specifications may well indicate that certain embodiments are preferred, particular embodiments appearing in a specification will not be read into the claims when the claim language is broader than such embodiments.").

Plaintiff also points to portions of the specification that require functionality that Plaintiff claims can only be performed by a split-gate transistor. *See, e.g.*, col. 1:41–2:9 (discussing the Kynett reference and explaining that its "floating gate extends from the source to the drain"). But the sections Plaintiff points out do not amount to disclaimers that override the plain meaning of the disputed term. *Computer Docking Station Corp. v. Dell, Inc.*, 519 F.3d 1366, 1375 (Fed. Cir. 2008) ("Prosecution disclaimer does not apply to an ambiguous disavowal."). For example, following the discussion of the Kynett article, the applicant listed proposed improvements over

the transistor discussed in Kynett. These improvements did not reference the position of the floating gate in relation to the channel. Col. 2:10–21.

Furthermore, the Court finds compelling that the specification says one embodiment "typically incorporates" a split-gate configuration. Col. 2:57-64. This permissive language belies the proposition that the split-gate structure is a necessary element of each claim.

Plaintiff also turns to the prosecution history to support its position. Plaintiff argues that the phrase "at least a portion of" was added to Claim 1 to distinguish the present invention from the prior art. Specifically, the examiner rejected Claim 1 as readable on U.S. Patent No. 4,628,487 (Smayling) (2:10-cv-207, Doc. No. 684-14 at 2). Plaintiff claims the language was added to distinguish Smayling, which included a stacked gate configuration. But, as Defendants point out, when the examiner rejected Claim 1, the disputed term was already used in the claim language to describe the relationship between the floating gate and the channel—a key distinction between split-gate transistors and non-split-gate transistors. Thus, the examiner understood a transistor with "a floating gate extending over at least a portion of said channel" to include Smayling's stacked gate. Furthermore, Plaintiff's amendment to Claim 1 to overcome the Smayling reference addressed the method of programming (hot electron injection versus tunneling), and thus, Plaintiff's argument is without merit (*see* Doc. No. 684-14 at 7).

Having considered the record and the parties' arguments and for the reasons discussed above, the Court construes the disputed term **"at least a portion of"** to mean **"any portion of up to and including the whole."**

B. "drain"/"drain region" and "source"/"source region"

Disputed Claim Term	'009	'719	'629	Plaintiff's Proposed Construction	Defendants' Proposed Construction
drain/drain region	1, 2, 4, 7, 8, 27, 28	1, 7	5	a doped single crystal silicon semiconductor substrate region that receives the charge carriers during the programming operation	a doped single crystal silicon semiconductor substrate region that receives the charge carriers during read and programming operations
source/source region	1, 2, 4, 7, 8, 27, 28	1, 7	5	a doped single crystal silicon semiconductor substrate region that is the origin of the charge carriers during the programming operation	a doped single crystal silicon semiconductor substrate region that is the origin of the charge carriers during read and programming operations

These terms appear in all three patents in suit, and the parties agree that the terms should have the same construction for all three patents. The parties also agree on the construction except as to one issue: whether the source and drain regions must serve the same role during both the programming and read operations. Plaintiff argues that the regions are defined by their operation only during programming, while Defendants claim that the regions must serve the same function during both operations. For the reasons discussed below, the Court rejects both positions and adopts the following construction for both terms: "a doped single crystal silicon semiconductor region of a floating gate transistor."

1. The Claim Language

Claim 1 of the '009 Patent is an exemplar claim that includes both disputed terms:

> A method for programming a floating gate transistor, said floating gate transistor comprising **a source**, **a drain** spaced apart from said **source**, said **source** and **drain** being of first conductivity type and formed in a semiconductor region of a second conductivity type, a channel extending between said **source** and **drain**, a floating gate extending over at least a portion of said channel, and

a control gate extending over at least a portion of said floating gate, said method comprising the steps of:

applying a programming voltage to said drain and control gate sufficient to cause hot electron injection programming of said transistor; and

ensuring that the programming drain current for said transistor is less than a predetermined value.

(emphasis added).

2. Court's Construction

Plaintiff argues that Defendants' position has no basis in the claim language, specification, or elsewhere in the intrinsic record. Defendants respond that the applicant affirmatively disclaimed a transistor where the source and drain regions were interchangeable. Defendants also note that the specification only describes embodiments where the source and drain regions are not interchangeable.

Both parties' constructions include method of use limitations related to the structural elements "drain" and "source." But the claims do not include method of use limitations. *See Mattox v. Infotopia, Inc.*, 136 F. App'x 366, 369 (Fed. Cir. 2005) (rejecting a court's claim construction "because it fail[ed] to respect that the claim language defines a structural element, not a method of use"). Accordingly, the Court will not include these in the construction.

Furthermore, Defendants' argument to read in limitations from the preferred embodiments is without merit. *Electo Med. Sys., S.A.*, 34 F.3d at 1054. Similarly, Defendants overstate the disclaimer in the prosecution history. The applicant distinguished the combination of the McElroy and Miccoli references by their lack of "asymmetry in the split gate EPROM" (2:10-cv-207, Doc. No. 685-2 at 184–85). This is not a clear and unequivocal disclaimer that the drain and source regions cannot reverse roles between the program and read functions. *See Computer Docking Station Corp.*, 519 F.3d at 1375.

Having considered the record and the parties' arguments and for the reasons discussed above, the Court construes the disputed terms **"drain"/"drain region"** and **"source"/"source region"** to mean **"a doped single crystal silicon semiconductor region of a floating gate transistor."**

C. "ensuring that the programming drain current for said transistor is less than a predetermined value"

Disputed Claim Term	'009	'719	'629	Plaintiff's Proposed Construction	Defendants' Proposed Construction
ensuring that the programming drain current for said transistor is less than a predetermined value	1, 2, 4, 7, 8, 27, 28			ensuring [alternatively, controlling] that the programming drain current is such that it is at a value below that which can be supplied by an on-chip current supply, such as a charge pump	ensuring that the programming drain current for said transistor is less than a predetermined value when hot electrons are being injected to program the transistor
ensuring	1, 2, 4, 7, 8, 27, 28			plain and ordinary meaning, alternatively "controlling"	making certain
programming drain current	1, 2, 4, 7, 8, 27, 28			current that flows through the channel during the programming operation	drain current that flows through the floating gate transistor when hot electrons are being injected to program the transistor
less than a predetermined value	1, 2, 4, 7, 8, 27, 28			below that which can be supplied by an on-chip current supply, such as a charge pump	less than a drain current value determined before hot electron injection programming occurs

This phrase only appears in Claim 1 of the ’009 Patent, and it amounts to the entire second step of the claimed method. According to Plaintiff, it “is the key to the invention” (Doc. No. 684 at 25). The fundamental dispute between the parties regarding this phrase is whether the predetermined value of the drain current is defined by what an on-chip power supply can provide. According to Plaintiff, this features is what made the ’009 Patent novel. Defendants counter that Plaintiff is attempting to read in a claim limitation from the embodiments in the specification.

Other disputes between the parties regarding this phrase include the following: (1) whether the current flows through the transistor or just the channel, (2) whether “programming” refers only to hot electron injection programming or any type of programming, (3) the meaning of “ensuring,” and (4) when the “ensuring” must occur.

For the reasons discussed below, the Court adopts Defendants’ construction: “making certain that the drain current that flows through the floating gate transistor when hot electrons are being injected to program the transistor is less than a drain current value determined before hot electron injection programming occurs.”

1. The Claim Language

Claim 1 of the ’009 Patent is an exemplar claim that includes the disputed phrase:

> A method for programming a floating gate transistor, said floating gate transistor comprising a source, a drain spaced apart from said source, said source and drain being of first conductivity type and formed in a semiconductor region of a second conductivity type, a channel extending between said source and drain, a floating gate extending over at least a portion of said channel, and a control gate extending over at least a portion of said floating gate, said method comprising the steps of:
>
> applying a programming voltage to said drain and control gate sufficient to cause hot electron injection programming of said transistor; and
>
> **ensuring that the programming drain current for said**

transistor is less than a predetermined value.

(emphasis added).

2. Court's Construction

The primary dispute as to this phrase is whether an on-chip power supply sets the benchmark for what is a "predetermined value." Plaintiff cites to several descriptions of embodiments that state that the power supply is on-chip. According to Plaintiff, the necessary construction of "predetermined value" is limited by the amount of current that an on-chip power supply can provide. Plaintiff claims that to construe otherwise would read the claims completely out of context and would strip the claims of their inventive properties.

Defendants respond that the term should be given its plain and ordinary meaning: determined beforehand, i.e. determined before hot electron injection programming. Although Defendants agree that the '009 Patent contemplates a power source that *can be* on-chip, it is not a required limitation that should be read into the term "predetermined value." Furthermore, Defendants note that Claim 4 limits the power source to a charge pump. If an on-chip charge pump is required for every claim, as Plaintiff's construction requires, then Claim 4 would add no new limitations, in violation of the claim differentiation principle. *See Curtiss-Wright Flow Control Corp. v. Velan, Inc.*, 438 F.3d 1374, 1380 (Fed. Cir. 2006) ("[A] dependent claim must add a limitation to those recited in the independent claim.").

The Court agrees with Defendants that Plaintiff has not demonstrated a compelling reason to import the preferred embodiments as limitations in the claims. Plaintiff also fails to demonstrate that the applicant made a clear statement intending to apply a construction different from the plain and ordinary meaning. Accordingly, the Court will apply the ordinary meaning of "predetermined value." *See Elektra Instr. v. O.U.R. Scientific Int'l, Inc.*, 214 F.3d

1302, 1307 (Fed. Cir. 2000) ("Absent an express intent to impart a novel meaning, claim terms take on their ordinary meaning.").

Regarding the "programming drain current" term, Defendants argue it must run through the transistor, while Plaintiff insists it only runs through the channel. The parties also dispute whether this relates only to hot electron injection programming or any type of programming (including tunneling), with Defendants proposing to limit it to hot electron injection programming. Defendants point to the repeated reference in the specification to support its position that the current must run through the transistor. *See*, *e.g.*, col 2:55–56. Plaintiff counters that, elsewhere, the specification cites to a current that runs from the source to drain, or through the channel. *See*, *e.g.*, col. 3:15–18. The Court finds that Defendants' construction more accurately reflects the meaning of "drain current" as discussed in the specification, rather than a "channel current."

Furthermore, Defendants look to the claim language itself to demonstrate that the claims are limited to hot electron injection programming. Specifically, the first step listed in Claim 1 refers exclusively to hot electron injection programming. Plaintiff appears to agree that the claims only apply to hot electron injection programming. But Plaintiff challenges the scope of when hot electron injection programming starts. Plaintiff claims Defendants' construction is improperly limited to the time when hot electrons are being injected and excludes the immediately preceding step of applying the voltage. Plaintiff argues that because the first step references "applying the voltage" that programming occurs before the hot electrons are injected. Plaintiff also refers to one of the preferred embodiments as supporting its position. *See* col. 7:30–60. But the Court finds uncompelling Plaintiff's argument that hot electron injection programming is broader than the act of programming, i.e. when hot electrons

are injected for programming.

The next issue raised by the parties pertains to the degree of certainty required by the term "ensuring." Plaintiff suggests a meaning synonymous with "controlling," which would allow for some variance in the actual application.[2] Defendants propose that "make certain" is the proper construction, which imposes the much stricter requirement that the voltage *actually* remain below the predetermined value.

Plaintiff looks to Claim 7, which states that the ensuring step "comprises the step of applying a voltage to said control gate to keep the drain current below said predetermined value." Plaintiff also notes that Claim 9 states the ensuring step "comprises the step of providing an electrical resistance between said source and ground." Plaintiff notes that both of these are consistent with its proposed construction that "ensuring" means applying some type of control with the goal of limiting the programming drain current. Plaintiff also turns to extrinsic evidence: the statement of its expert that requiring the current to *actually* stay below a predetermined amount is not practical in real-world application.

Defendants respond that their proposed construction—"make certain"—is consistent with the plain meaning of "ensuring." Defendants also cite several references in the specification where "ensure" or "ensuring" is used to mean "make certain." *See, e.g.*, col. 2:51–57. Defendants also point to several places in the specification stating that the invention does not function if the drain current exceeds a certain amount, *see, e.g.*, col. 2:48–50 ("there is no period of time during which the drain current exceeds a value greater than that which the charge pump can supply"). Defendants also note that Plaintiff's expert testimony addresses the manufacturing process, not programming the transistor.

[2] Plaintiff proposes that the term needs no construction on the basis that its plain and ordinary meaning is consistent with a construction of "controlling." Alternatively, Plaintiff proposes construing the term to mean "controlling."

The Court agrees that the specification clarifies that the ensuring step mandates *actually* maintaining the programming drain current below a certain value, not just applying controls with the *goal* of limiting the value of the drain current.

Finally, the parties dispute whether the ensuring step must occur when the hot electrons are being injected for programming or if it can also be performed at the time the voltage is applied to the drain and control gates. For the reasons previously discussed, the Court finds that the ensuring step must occur during programming, i.e. when the hot electrons are being injected for programming.

Having considered the record and the parties' arguments and for the reasons discussed above, the Court construes the disputed term **"ensuring that the programming drain current for said transistor is less than a predetermined value"** to mean **"making certain that the drain current that flows through the floating gate transistor when hot electrons are being injected to program the transistor is less than a drain current value determined before hot electron injection programming occurs."**

D. "erase gate"/"said method further comprising raising the voltage at said erase gate"

Disputed Claim Term	'009	'719	'629	Plaintiff's Proposed Construction	Defendants' Proposed Construction
erase gate	8			a gate which removes charge from the floating gate to facilitate erasing of a cell	a gate provided in addition to and separate from the control gate that is used in removing charge from the floating gate and also used to enhance programming efficiency during hot electron programming
said method further comprising raising the voltage at said erase gate	8			*See* construction of "erase gate" No further construction necessary.	raising the voltage of the erase gate when hot electrons are being injected to program the transistor

These terms present three issues in dispute: (1) whether the erase gate must be distinct from the control gate, (2) whether the erase gate must enhance programming efficiency, and (3) whether the construction should explicitly state that the voltage at the erase gate must be raised when the hot electrons are being injected for programming.

For the reasons discussed below, the Court rejects both positions and adopts the following construction for "erase gate": "a gate provided in addition to and separate from the control gate, which is capable of removing charge from the floating gate." The Court finds no construction is necessary for the term "said method further comprising raising the voltage at said erase gate."

1. The Claim Language

Claim 8 of the '009 Patent is an exemplar claim that includes both disputed terms:

> Method of claim 7 wherein said transistor comprises an **erase gate** capacitively coupled to said floating gate, **said method further comprising the step of raising the voltage at said erase gate**.
>
> (emphasis added).

2. Court's Construction

Defendant argues that the erase gate and control gate must be distinct features of the claimed invention. Defendants note that the claims identify two structures—the control and erase gates—performing two different functions. According to Defendants, this requires the two gates to be distinct. Defendant also points to the description of the erase gate function in the specification: "to enhance programming efficiency." Defendants argue that in order to perform the erase gate function listed in the specification, the erase and control gates must be separate. Plaintiff counters with a construction it claims coincides with the well-known meaning in the field of technology.

The recitation in the claims of two separate structural limitations does not require separate control and erase gates. *See Intel Corp. v. Int'l Trade Comm'n*, 946 F.2d 821, 832 (Fed. Cir. 1991). But Claim 8 requires that, during programming (pursuant to the preamble to Claim 1, on which Claim 8 depends via Claim 7), the programming voltage must be applied to the control gate. Furthermore, the voltage is raised at the erase gate, "typically during programming." Col. 7:67–8:2. The device must have an erase gate separate from the control gate to realize such an operation. *See Inpro II Licensing, S.A.R.L. v. T-Mobile USA, Inc.*, 450 F.3d 1350, 1354–55 (Fed. Cir. 2006). Accordingly, Defendant's proposed limitation is supported by the intrinsic record.

Defendants also argue that the erase gate must be used to enhance programming efficiency. The specification describes such use of the erase gate, but the claims do not. Accordingly, Defendant's construction would improperly import a use limitation into the construction, effectively requiring an additional "using . . ." step. This is not supported by the claim language.[3]

Finally, Defendants argue that the voltage must be increased when hot electron programming occurs. Defendant claims that the method step claimed in dependent Claim 8 refers to the hot electron injection programming from Claim 1. But the method recited in the preamble of Claim 1 is a method for programming not limited to hot electron injection programming. The hot electron programming is introduced in the "applying a programming voltage" step. Thus, the method referred to in Claim 8, is not limited to hot electron injection programming. Defendants cite no further basis for importing the temporal limitation that the voltage at the erase gate must be raised when (rather than before) hot electrons are being injecting into the floating gate.

Having considered the record and the parties' arguments and for the reasons discussed

[3] Similarly, both parties propose importing a limitation that the erase gate be used to remove charge from the floating gate. The Court has modified the construction to state that the erase gate must be *capable* of removing the charge from the floating gate.

above, the Court construes the dispute term **"erase gate"** to mean **"a gate provided in addition to and separate from the control gate, which is capable of removing charge from the floating gate."** The Court further determines that the phrase **"said method further comprising the step of raising the voltage at said erase gate**" does not need to be construed.

E. "split gate transistor"

Disputed Claim Term	'009	'719	'629	Plaintiff's Proposed Construction	Defendants' Proposed Construction
split gate transistor		1, 7		memory cell in which the floating gate extends over only a portion of the channel	a transistor that has a floating gate and a control gate

The issue in dispute regarding this term is whether "split gate" should be defined by the position of the floating gate in relation to the channel. Plaintiff claims that the ordinary meaning of "split-gate transistor" demands that such a limitation be included in the construction. Defendants propose a much broader construction that merely requires the transistor to have a control gate and a floating gate. For the reasons discussed below, the Court rejects both positions and adopts the following construction: "a transistor having a control gate overlapping a floating gate such that a non-symmetrical arrangement of the control gate and floating gate are created and where the floating gate extends over only a portion of the channel."

1. The Claim Language

Claim 1 of the '719 Patent is an exemplar claim that includes the disputed term:

> A method of manufacturing a memory cell containing a **split gate transistor** comprising:
> forming first polycrystalline silicon on, but separated from a semiconductor substrate by first insulation, said first polycrystalline silicon defining a floating gate having a first edge and a second edge opposite said first edge;
> forming a photoresist pattern over said substrate and over a surface of said first polycrystalline silicon, said surface

> extending laterally between the first and second edges, a first opening being formed in said photoresist pattern to expose both the first edge of said floating gate and a first portion of the semiconductor substrate extending laterally from said first edge and a second opening being formed in said photoresist pattern to expose a second portion of the semiconductor substrate laterally spaced apart from said floating gate;
>
> implanting selected impurities into those portions of the semiconductor substrate exposed by the openings of said photoresist thereby to form a source region laterally spaced apart from said floating gate and a drain region extending from but self-aligned to the first edge of said floating gate.

(emphasis added).

2. Court's Construction

Plaintiff recites a construction that it claims is consistent with the ordinary meaning of the term "split gate transistor." Plaintiff claims its argument is bolstered by the fact that every embodiment as well as the extrinsic evidence (including Defendants' expert) is consistent with Plaintiff's construction. Defendants respond by citing a portion of the specification that states "[t]his invention relates to a nonvolatile . . . EPROM having a split gate (i.e., both a floating gate and a control gate)." Referring to this statement, Defendants note that language following "i.e." is considered an express definition. *See Doyle v. Crain Indus., Inc.*, 243 F.3d 564, 564 (Fed. Cir. 2000) (unpublished table decision).

The Court is not convinced that the unpublished case cited by Defendants that references the distinction between "e.g." and "i.e." overrides the longstanding principle that the applicant must clearly manifest an intent to act as his own lexicographer. *See Merck & Co., Inc. v. Teva Pharm. USA, Inc.*, 395 F.3d 1364, 1370 (Fed. Cir. 2005) ("When a patentee acts as his own lexicographer if redefining the meaning of particular claim terms away from their ordinary meaning, he must clearly express that intent in the written description."). The parties agree that a split gate transistor includes both a control gate and a floating gate. The dispute is whether that is

the *only* limitation. Defendant has pointed to nothing in the claims or extrinsic evidence to support the applicant's redefining the term.

But Plaintiff improperly focuses its construction solely on the relationship between the floating gate and the channel. The more relevant relationship is between the floating gate and the control gate. The specification makes this clear in describing the Harari prior art, which was a split gate structure. Fig. 2, col. 1:21–51. Accordingly, the Court incorporates the relationship between the floating gate and the control gate—as described in the specification—into the construction of "split gate."

Defendant also argues that Plaintiff—without support in the intrinsic evidence—conflates the terms "transistor" and "memory cell." The Court agrees.

Having considered the record and the parties' arguments and for the reasons discussed above, the Court construes the disputed term **"split gate transistor"** to mean **"a transistor having a control gate overlapping a floating gate such that a non-symmetrical arrangement of the control gate and floating gate are created and where the floating gate extends over only a portion of the channel."**

F. "self-aligned"/"aligned"

Disputed Claim Term	'009	'719	'629	Plaintiff's Proposed Construction	Defendants' Proposed Construction
self-aligned		1, 7		formed by alignment to the edge of the floating gate, using the floating gate as a mask, such that the channel length under the floating gate will be defined by the floating gate itself regardless of any processing misalignments	the portion of the transistor channel length under the floating gate will be defined by the floating gate itself regardless of any processing misalignment thereby ensuring a constant channel length under the floating gate

aligned			5	formed by alignment to the edge of the floating gate, using the floating gate as a mask, such that the channel length under the floating gate will be defined by the floating gate itself regardless of any processing misalignments	placed or laid in a line

Both parties look to the express definition of "self-aligned" in the specification. But they dispute how much of the specification's language should be incorporated into the construction. Furthermore, Plaintiff proposes the same construction for "aligned," while Defendant argues that the terms should be construed differently.

For the reasons discussed below, the Court adopts Defendants' constructions. The Court construes "self-aligned" to mean "the portion of the transistor channel length under the floating gate will be defined by the floating gate itself regardless of any processing misalignment thereby ensuring a constant channel length under the floating gate." The term "aligned" is construed as "placed or laid in a line."

1. The Claim Language

Claim 1 of the '719 Patent is an exemplar claim that includes the disputed term "self-aligned":

> A method of manufacturing a memory cell containing a split gate transistor comprising:
>
> forming first polycrystalline silicon on, but separated from a semiconductor substrate by first insulation, said first polycrystalline silicon defining a floating gate having a first edge and a second edge opposite said first edge;
>
> forming a photoresist pattern over said substrate and over a surface of said first polycrystalline silicon, said surface extending laterally between the first and second edges, a first opening being formed in said photoresist pattern to expose both

> the first edge of said floating gate and a first portion of the semiconductor substrate extending laterally from said first edge and a second opening being formed in said photoresist pattern to expose a second portion of the semiconductor substrate laterally spaced apart from said floating gate;
>
> implanting selected impurities into those portions of the semiconductor substrate exposed by the openings of said photoresist thereby to form a source region laterally spaced apart from said floating gate and a drain region extending from but **self-aligned** to the first edge of said floating gate.

(emphasis added).

2. Court's Construction

In the specification, the applicant states:

> By "self-aligned" I mean that the portion of the transistor channel length under the floating gate will be defined by the floating gate itself regardless of any processing misalignments thereby insuring a constant channel length under the floating gate. To do this, a special process is employed wherein the floating gate is used to define one edge of the drain region.
>
> The '719 Patent, col. 3:50–56.

The parties agree this is an express definition of "self-aligned." But Defendants claim the definition stops with the first sentence, and Plaintiff claims both sentences are a part of the definition. But the second sentence refers to *how* the floating gate is self-aligned. It does not define the term itself. Plaintiffs' construction also introduces the term "mask," which is not drawn from this express definition.

Additionally, Plaintiff has offered no support for its position that the two terms—"self-align" and "aligned"—should be given the same meaning. *See Acumed LLC v. Stryker Corp.*, 483 F.3d 800, 807 (Fed. Cir. 2007) (relying on principle that different words in patent claims are presumed to have different meanings). In the absence of any other basis for an alternative definition, the Court applies the ordinary meaning of "aligned": "placed or laid in a line."

Having considered the record and the parties' arguments and for the reasons discussed above, the Court construes the dispute term **"self-aligned"** to mean **"the portion of the transistor channel length under the floating gate will be defined by the floating gate itself regardless of any processing misalignment thereby ensuring a constant channel length under the floating gate."** The Court further determines that **"aligned"** means **"placed or laid in a line."**

G. "photoresist pattern"/" forming a photoresist pattern over said substrate and over a surface of said first polycrystalline silicon"/"forming a photo-resistive coating on the floating gate of each transistor"

Disputed Claim Term	'009	'719	'629	Plaintiff's Proposed Construction	Defendants' Proposed Construction
photoresist pattern		1		the pattern that is made by removing portions of the photoresist material	the pattern that is made in a photoresist coating by removing portions of the photoresist material
forming a photoresist pattern over said substrate and over a surface of said first polycrystalline silicon		1		"**over said substrate**" means "above the substrate" "**over a surface of said first polycrystalline silicon**" means "above the area of the floating gate that extends laterally between the first and second edges of the floating gate"	forming a photoresist pattern upon an upper or top surface of the first polycrystalline silicon and the substrate before forming the insulating oxide layer or second polycrystalline silicon layer for the control gate
forming a photo-resistive coating on the floating gate of each transistor		7		applying a photoresist coating on each of the floating gates. This limitation does not require that the coating to be on the entire floating gate extending from its first edge to its second edge	forming a photoresistive coating in contact with the top surface of the floating gate of each transistor before forming the insulating oxide layer or second polycrystalline silicon layer for the control gate

The parties' dispute centers on whether the claimed process precludes inclusion of layers not expressly recited in the claims. Plaintiff insists that the claims allow additional layers. Defendants call for the more narrow construction. For the reasons discussed below, the Court adopts Defendants' constructions.

1. The Claim Language

Claim 1 of the '719 Patent is an exemplar claim that includes the disputed phrase "forming a photoresist pattern over said substrate and over a surface of said first polycrystalline silicon":

> A method of manufacturing a memory cell containing a split gate transistor comprising:
>
> forming first polycrystalline silicon on, but separated from a semiconductor substrate by first insulation, said first polycrystalline silicon defining a floating gate having a first edge and a second edge opposite said first edge;
>
> **forming a photoresist pattern over said substrate and over a surface of said first polycrystalline silicon**, said surface extending laterally between the first and second edges, a first opening being formed in said photoresist pattern to expose both the first edge of said floating gate and a first portion of the semiconductor substrate extending laterally from said first edge and a second opening being formed in said photoresist pattern to expose a second portion of the semiconductor substrate laterally spaced apart from said floating gate;
>
> implanting selected impurities into those portions of the semiconductor substrate exposed by the openings of said photoresist thereby to form a source region laterally spaced apart from said floating gate and a drain region extending from but self-aligned to the first edge of said floating gate.

(emphasis added).

2. Court's Construction

Defendants' proposed constructions all preclude additional layers—whether insulating oxide or additional photoresist–when not expressly recited in the claims. Defendants look primarily to the prosecution history, arguing that the applicant expressly disclaimed the inclusion of an additional oxide layer between the first polycrystalline silicon (i.e., the floating

gate) and the photoresist pattern or coating. Defendants also point to a disclosure in the specification where the applicant states that the photoresist layer is formed on top of the floating gate polycrystalline silicon. See col. 5:9–13. Similarly, Defendants note that the specification states that the photoresist pattern is formed in a photoresist coating, not in some other material, as there would be if there were multiple photoresist layers.

Plaintiff counters that Defendants' construction violates the tenet that "comprising" does not preclude steps that are not recited in the claim. *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 811 (Fed. Cir. 1999). Plaintiff further claims that Defendants improperly attempt to incorporate a preferred embodiment as a limitation. Finally, Plaintiff argues that Defendant overstates the prosecution history.

As noted by the parties, the term "over" has a broad meaning (i.e., above the surface and thus not in direct contact) and a narrow meaning (i.e., on the surface and thus in direct contact). Where the intrinsic evidence does not indicate otherwise, the preference is for the narrower construction. See *Athletic Alts., Inc. v. Prince Mfg., Inc.*, 73 F.3d 1573, 1581 (Fed. Cir. 1996).

Furthermore, during prosecution, application Claim 8, which was renumbered to be issued as Claim 1, was amended to recite that a photoresist pattern is formed "over said substrate and over a surface of said [floating gate]." Def.'s Resp., Ex. 18 at 1–2. In remarks, the applicant distinguished the Iizuka reference by saying that in the present invention "there is no poly oxide layer covering poly layer 52 when the source and drain regions are implanted." *Id.* at 9–10. The layer 52 refers to the floating gate. The only limitation in Claim 8 that provided a basis for applicant's remark was the amendment that the photoresist pattern is "over said substrate and over a surface of said [floating gate]." In the context of applicant's remarks, the limitation means that the layer of photoresist material is placed on the upper or top surface of the floating gate.

Accordingly, the Court adopts Defendant's constructions that limits the use of "over" and "on" the substrate and floating gate (or first polycrystalline silicon) to mean "in direct contact with."

Having considered the record and the parties' arguments and for the reasons discussed above, the Court construes the disputed term **"photoresist pattern"** to mean **"the pattern that is made in a photoresist coating by removing portions of the photoresist material."** The Court further determines that the phrase **"forming a photoresist pattern over said substrate and over a surface of said first polycrystalline silicon"** means **"forming a photoresist pattern upon an upper or top surface of the first polycrystalline silicon and the substrate before forming the insulating oxide layer or second polycrystalline silicon layer for the control gate."**

H. "to expose"/"exposed"

Disputed Claim Term	'009	'719	'629	Plaintiff's Proposed Construction	Defendants' Proposed Construction
to expose		1,7		to leave an area without photoresist	to leave uncovered or unprotected by any layer or material, such as an oxide layer
exposed		1, 7		not covered by photoresist	uncovered or unprotected by any layer or material, such as an oxide layer

Like the previous terms, the parties here dispute the relationship required between the various layers when manufacturing the transistor. In this instance, Plaintiff claims that only the photoresist layer must be removed to "expose" an area for the source and drain regions. Defendants argue that all layers must be removed down to the substrate. For the reasons discussed below, the Court adopts Defendants' constructions.

1. The Claim Language

Claim 1 of the '719 Patent includes the disputed terms:

> A method of manufacturing a memory cell containing a split gate transistor comprising:
>
> forming first polycrystalline silicon on, but separated from a semiconductor substrate by first insulation, said first polycrystalline silicon defining a floating gate having a first edge and a second edge opposite said first edge;
>
> forming a photoresist pattern over said substrate and over a surface of said first polycrystalline silicon, said surface extending laterally between the first and second edges, a first opening being formed in said photoresist pattern **to expose** both the first edge of said floating gate and a first portion of the semiconductor substrate extending laterally from said first edge and a second opening being formed in said photoresist pattern **to expose** a second portion of the semiconductor substrate laterally spaced apart from said floating gate;
>
> implanting selected impurities into those portions of the semiconductor substrate **exposed** by the openings of said photoresist thereby to form a source region laterally spaced apart from said floating gate and a drain region extending from but self-aligned to the first edge of said floating gate.

(emphasis added).

2. Court's Construction

Defendants argue that the ordinary meaning of "expose" applies: uncovered or unprotected. Defendants point to the claim language itself, the embodiments described in the patent, and the prosecution history as all consistent with their position. Plaintiff responds that Defendants are improperly reading in a limitation from the embodiment. Plaintiff notes that nothing in the intrinsic record states that the photoresist layer *and all other layers* must be removed, leaving bare the underlying structure (i.e., the substrate or the floating gate). Plaintiff also cites to expert statements indicating that its construction is consistent with common practice in the field at the time of the invention.

Plaintiff's proposed construction is inconsistent with the claim language. Plaintiff insists that "expose" simply means removing the photoresist layer. But the claims separately require the creation of the opening in the photoresist pattern. Plaintiff's definition would render the term

"exposed" superfluous, which is disfavored. *Creative Integrated Sys., Inc. v. Nintendo of Am., Inc.*, 526 F. App'x 927, 935 (Fed. Cir. 2013).

Having considered the record and the parties' arguments and for the reasons discussed above, the Court construes the dispute term **"to expose"** to mean **"to leave uncovered or unprotected by any layer or material, such as an oxide layer."** The Court further determines that **"exposed"** means **"uncovered or unprotected by any layer or material, such as an oxide layer."**

I. "effective channel length"

Disputed Claim Term	'009	'719	'629	Plaintiff's Proposed Construction	Defendants' Proposed Construction
effective channel length		7		the length of the channel under the floating gate after processing	the length of the channel under the floating gate

The only dispute regarding this term is whether to include "after processing" at the end of the construction as proposed by Plaintiff. For the reasons discussed below, the Court adopts Defendants' proposed construction.

1. The Claim Language

Claim 7 of the '719 Patent includes the disputed term:

> A manufacturing method for assuring consistency over process variations in the **effective channel length** of a plurality of split gate transistors which are to be formed each to have a floating gate laterally spaced apart from a source region of the transistor, the method comprising:
>
> insulatively disposing the floating gate of each transistor on a semiconductive substrate;
>
> forming a photoresistive coating on the floating gate of each transistor, the coating extending laterally beyond the floating gate to cover the substrate;
>
> creating a first opening in the coating to expose an edge portion of the floating gate of each transistor and a

> first portion of the substrate directly adjacent to the edge portion;
> creating a second opening in the coating, laterally spaced apart from the floating gate, to expose a second portion of the substrate; and
> implanting doping impurities through the first and second openings to create for each of the plurality of transistors a drain region which is self-aligned to the edge portion of the floating gate of the transistor and a source region which is spaced apart from the floating gate of the transistor.

(emphasis added).

2. Court's Construction

Plaintiff argues that the claim language, *see* col. 13:21–26, and the specification, *see, e.g.*, col. 6:55–60, both indicate that the "effective channel length" is the length under the channel *after processing*. Defendant argues that the "after processing" language would be confusing to the jury and also conflicts with embodiments in which additional processing is needed after creating the effective channel length, *see* col 3:67–4:14. The Court agrees that "after processing" adds ambiguity to the construction and is unnecessary.

Having considered the record and the parties' arguments and for the reasons discussed above, the Court construes the disputed term **"effective channel length"** to mean **"the length of the channel under the floating gate."**

V. CONCLUSION

For the forgoing reasons, the Court adopts the constructions as set forth above, and as listed in the attached chart. The parties are ordered that they may not refer, directly or indirectly, to each other's claim construction positions in the presence of the jury. Likewise, the parties are ordered to refrain from mentioning any portion of this opinion, other than the actual definitions adopted by the Court, in the presence of the jury. Any reference to claim construction proceedings is limited

to informing the jury of the definitions adopted by the Court.

It is SO ORDERED.

SIGNED this 3rd day of January, 2014.

MICHAEL H. SCHNEIDER
UNITED STATES DISTRICT JUDGE

APPENDIX A

Disputed Claim Term	'009	'719	'629	Court's Construction
at least a portion of	1, 2, 4, 7, 8, 27, & 28			any portion of up to and including the whole
drain/drain region	1, 2, 4, 7, 8, 27, & 28	1 & 7	5	a doped single crystal silicon semiconductor region of a floating gate transistor
source/source region	1, 2, 4, 7, 8, 27, & 28	1 & 7	5	a doped single crystal silicon semiconductor region of a floating gate transistor
ensuring that the programming drain current for said transistor is less than a predetermined value	1, 2, 4, 7, 8, 27, 28			making certain that the drain current that flows through the floating gate transistor when hot electrons are being injected to program the transistor is less than a drain current value determined before hot electron injection programming occurs
ensuring	1, 2, 4, 7, 8, 27, 28			making certain
programming drain current	1, 2, 4, 7, 8, 27, 28			the drain current that flows through the floating gate transistor when hot electrons are being injected to program the transistor
less than a predetermined value	1, 2, 4, 7, 8, 27, 28			less than a drain current value determined before hot electron injection programming occurs
erase gate	8			a gate provided in addition to and separate from the control gate, which is capable of removing charge from the floating gate

said method further comprising raising the voltage at said erase gate	8			plain and ordinary meaning
split gate transistor		1, 7		a transistor having a control gate overlapping a floating gate such that a non-symmetrical arrangement of the control gate and floating gate are created and where the floating gate extends over only a portion of the channel
self-aligned		1, 7		the portion of the transistor channel length under the floating gate will be defined by the floating gate itself regardless of any processing misalignment thereby ensuring a constant channel length under the floating gate
aligned			5	placed or laid in a line
photoresist pattern		1		the pattern that is made in a photoresist coating by removing portions of the photoresist material
forming a photoresist pattern over said substrate and over a surface of said first polycrystalline silicon		1		forming a photoresist pattern upon an upper or top surface of the first polycrystalline silicon and the substrate before forming the insulating oxide layer or second polycrystalline silicon layer for the control gate
forming a photo-resistive coating on the floating gate of each transistor		7		forming a photoresistive coating in contact with the top surface of the floating gate of each transistor before forming the insulating oxide layer or second polycrystalline silicon layer for the control gate
to expose		1,7		to leave uncovered or unprotected by any layer or material, such as an oxide layer

exposed		1, 7		uncovered or unprotected by any layer or material, such as an oxide layer
effective channel length		7		the length of the channel under the floating gate